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FIG. 1  
(PRIOR ART)

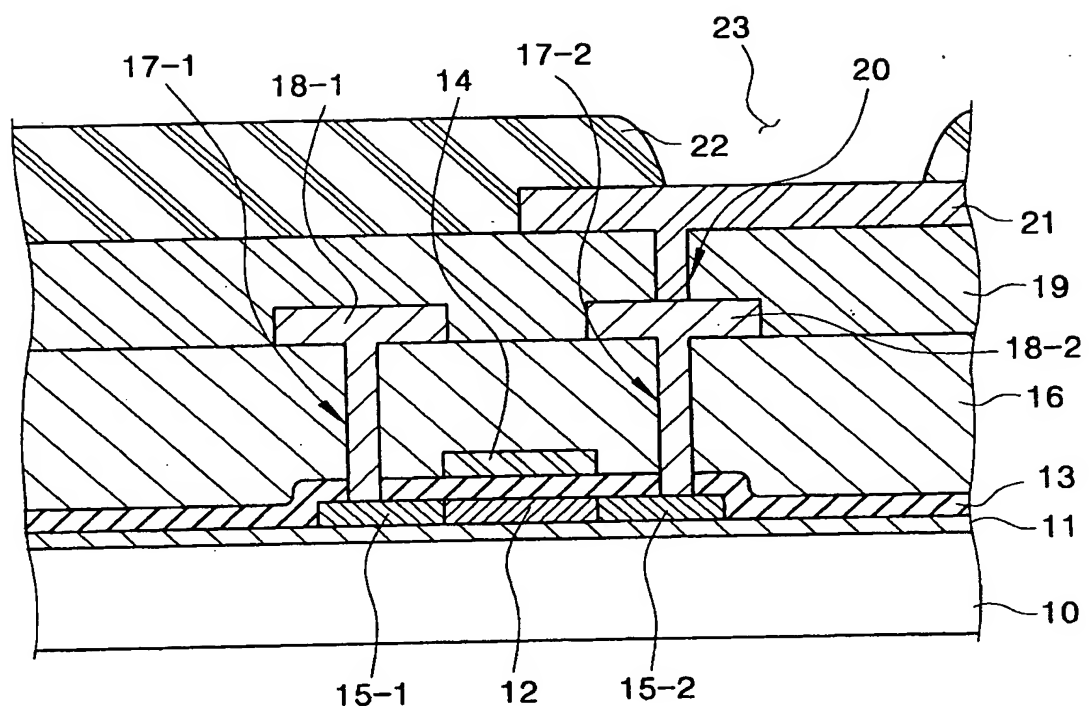


FIG. 2A

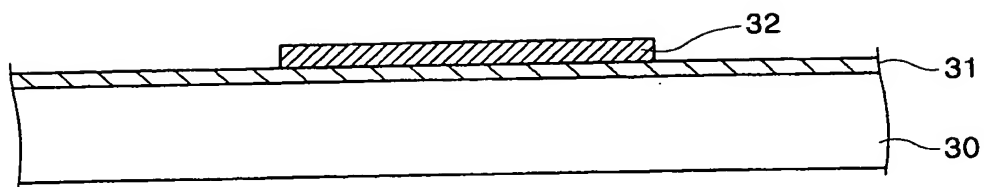


FIG. 2B

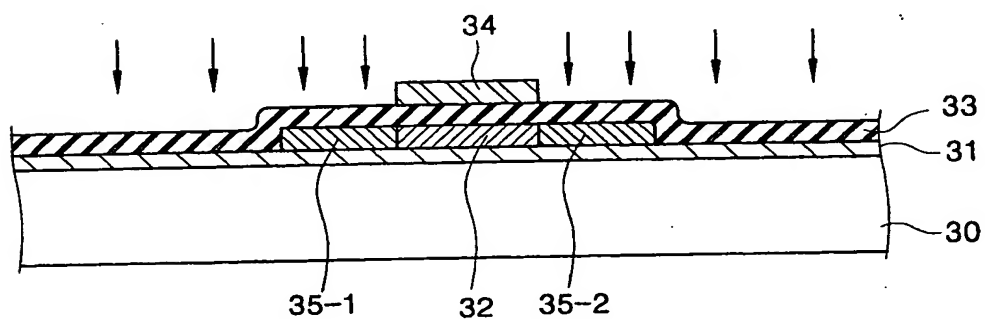


FIG. 2C

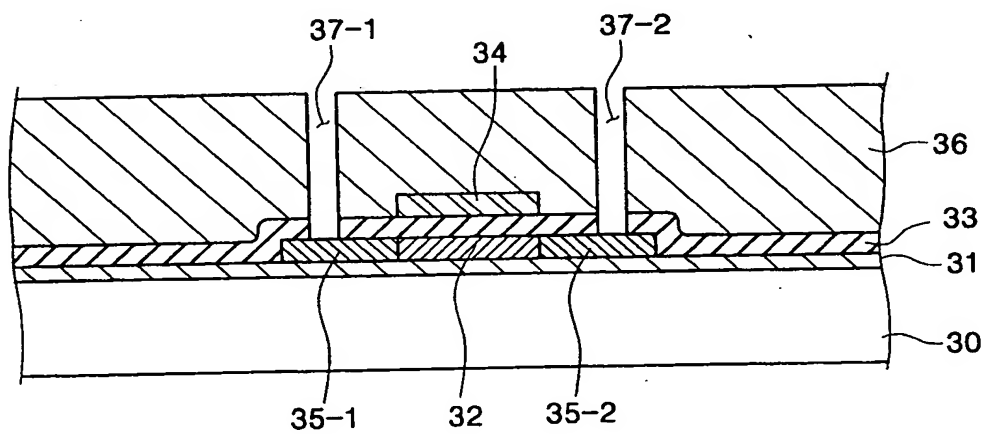


FIG. 2D

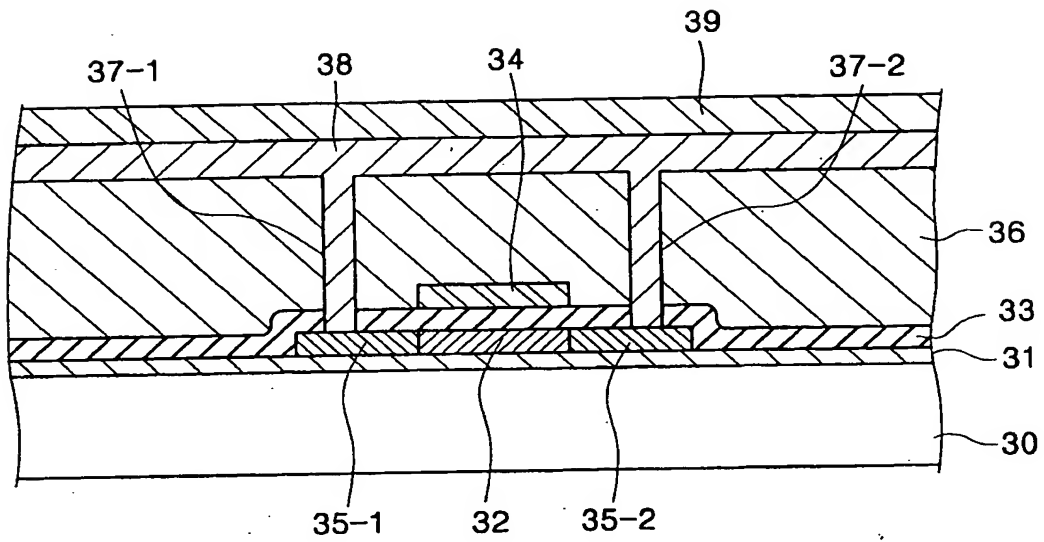


FIG. 2E

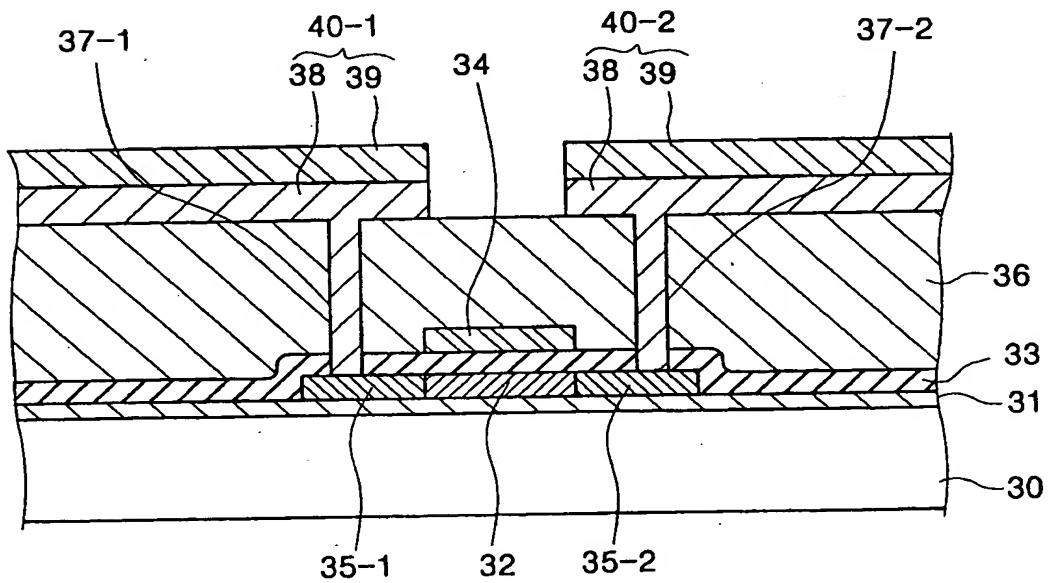


FIG. 3A

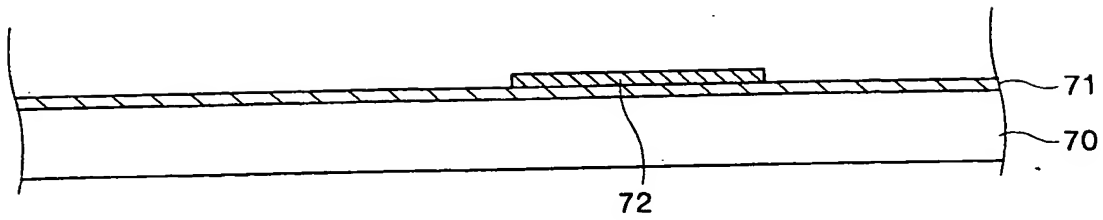


FIG. 3B

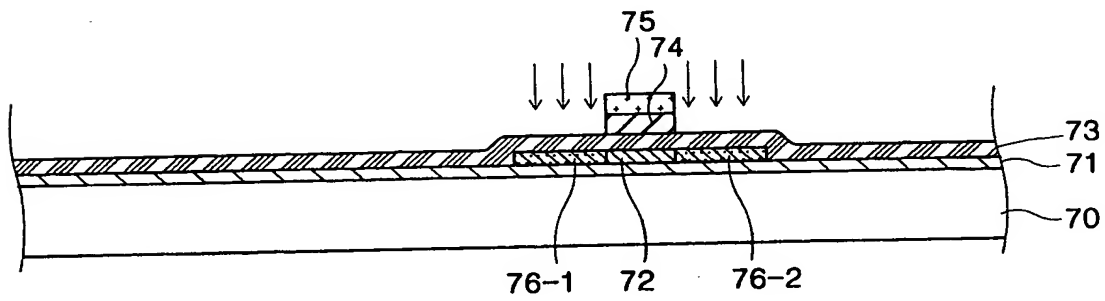


FIG. 3C

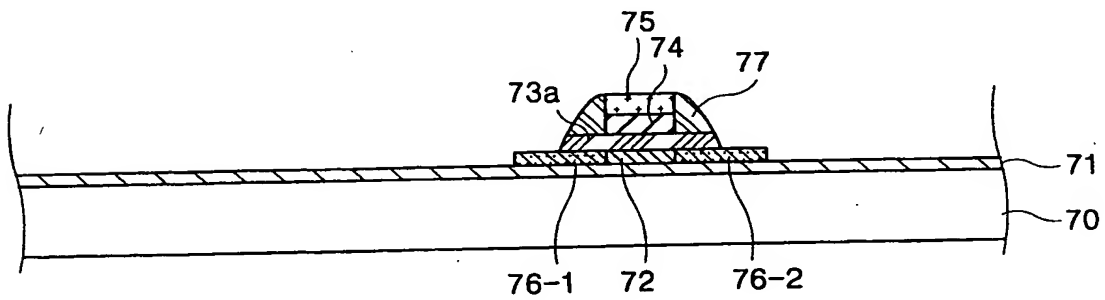


FIG. 3D

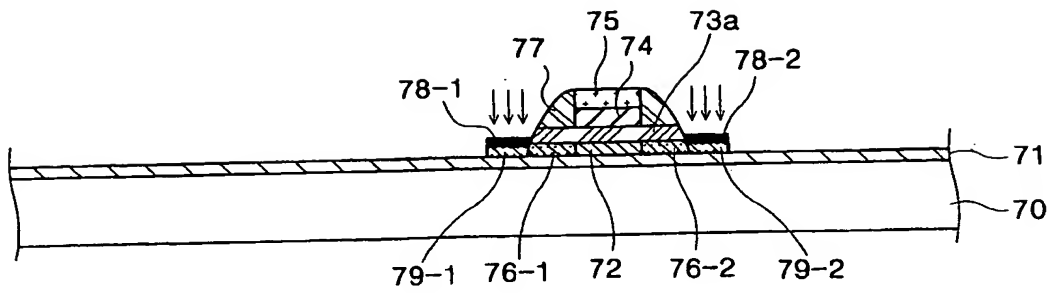


FIG. 3E

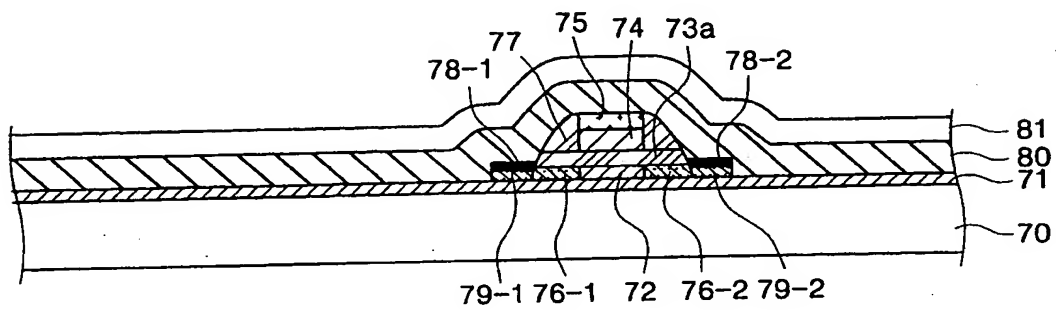


FIG. 3F

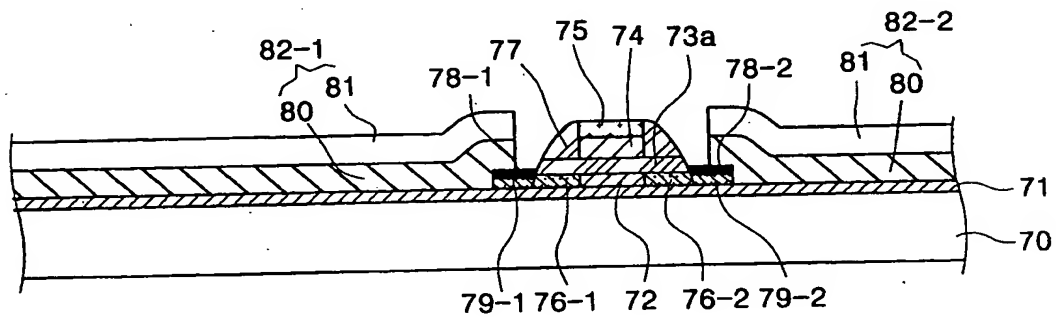


FIG. 4A

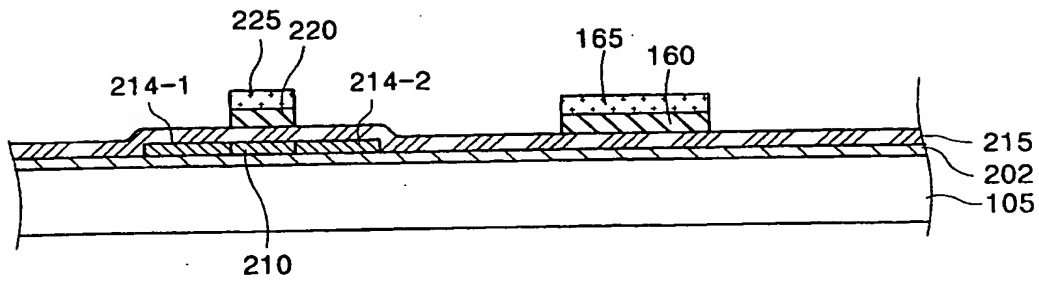


FIG. 4B

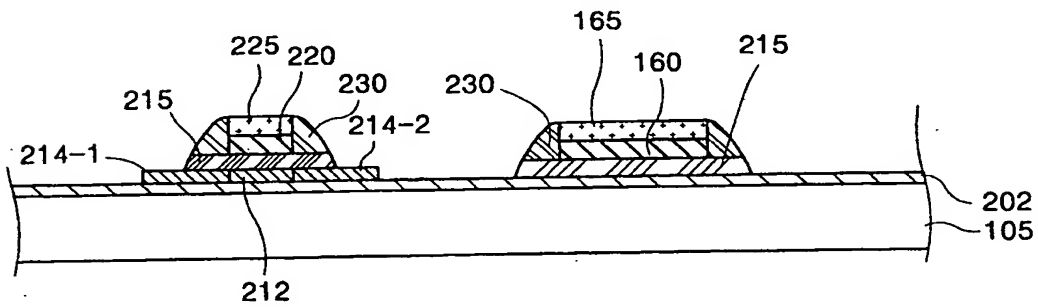


FIG. 4C

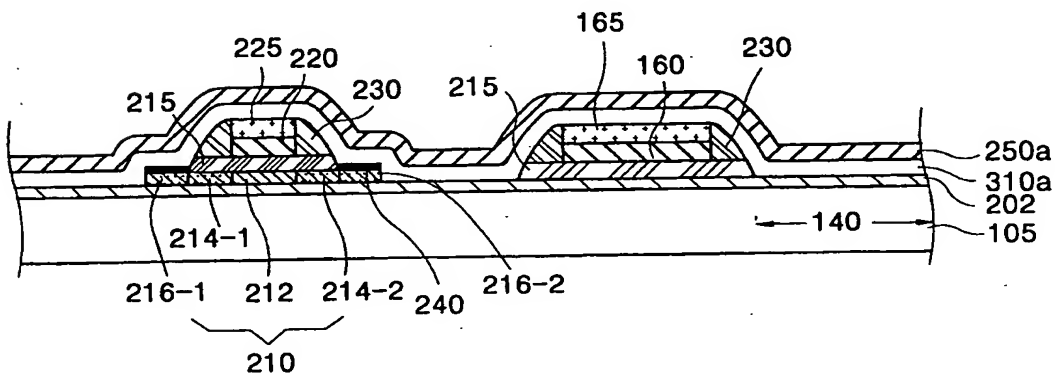


FIG. 4D

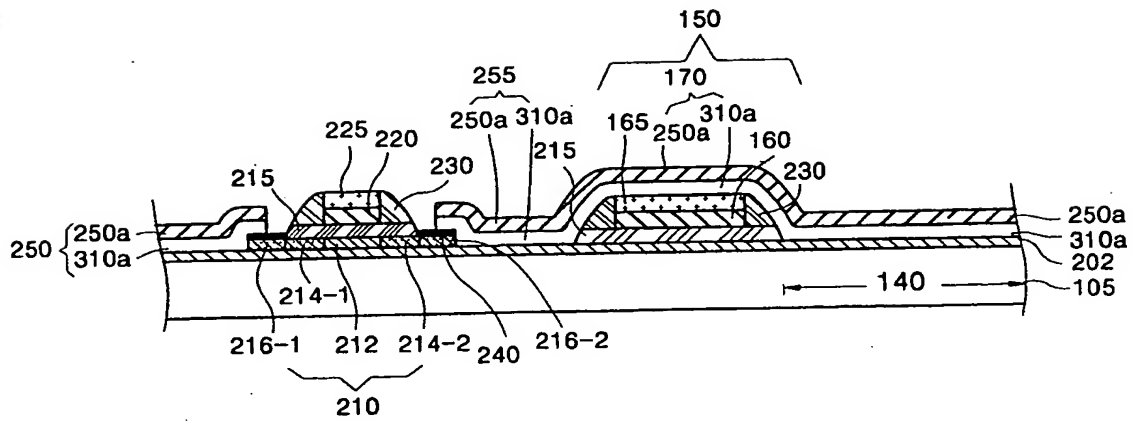
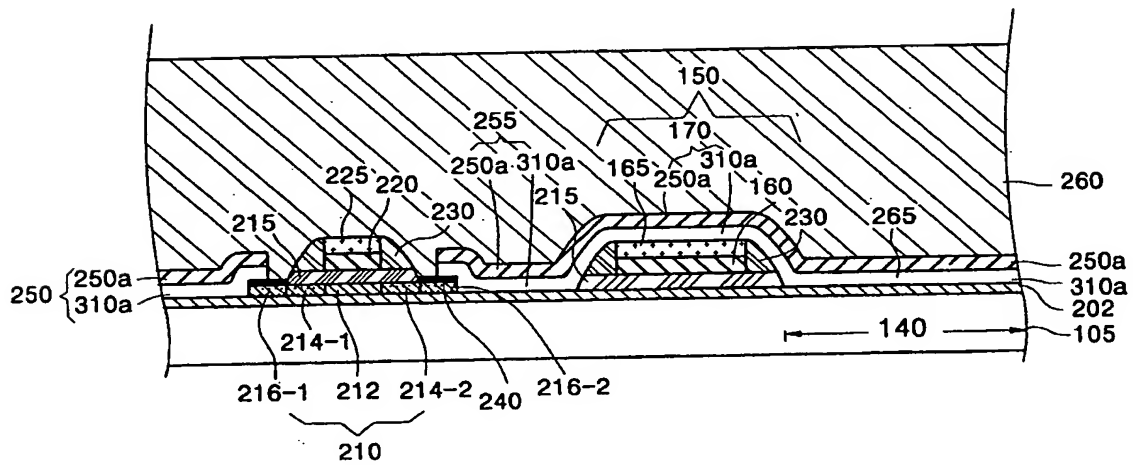


FIG. 4E





This cross-sectional view illustrates a semiconductor device. A substrate 105 is at the bottom, with a base layer 140 above it. The device features a central region 210 containing a stack of layers 212, 214-1, 214-2, 216-1, and 216-2. To the left of this central region is a structure 250 consisting of layers 250a and 310a, with a contact 215 and a pad 225. To the right is a more complex structure 260, also with layers 250a and 310a, featuring a contact 215, a pad 225, and a series of layers 150, 160, 165, 170, and 230. A layer 202 is positioned between the base layer 140 and the structures 250 and 260. A layer 266 is shown on the far right, and a layer 265 is located between the base layer 140 and the structure 260. Other labels include 220, 230, 240, 255, and 310a.

[illegible]

FIG. 5A

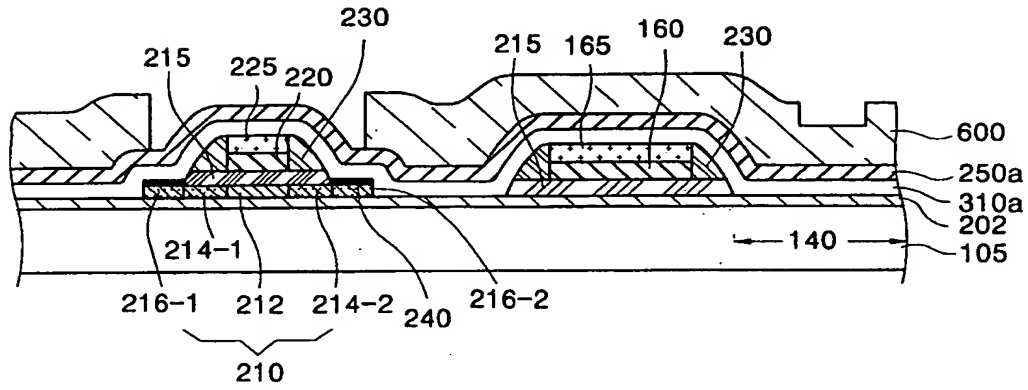


FIG. 5B

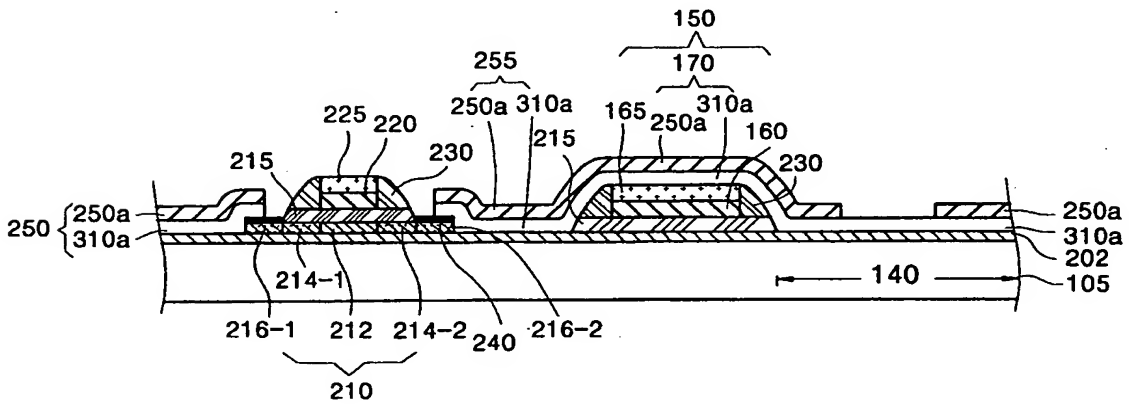


FIG. 5C

